Takashi Ichimori, Ph.D.

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Professional Summary

Engineering leader with deep experience in semiconductor process integration, thin-film deposition, silicide formation, SOI device engineering, and advanced failure analysis (TEM, FIB, SEM, EDS, XRD, XRF). Spent 18+ years at OKI / Lapis Semiconductor driving key innovations in Co-salicide, FeRAM capacitor processes, and plasma-etch defect mechanisms, supported by 45+ international patents and peer-reviewed publications.

Built strong real-world expertise in semiconductor equipment installation and factory integration, managing utilities, multi-vendor construction, tool move-in, hook-up, acceptance testing, and safe bring-up (ASM, Aixtron, Primaxx). Experienced in operational safety, gas-detection systems, fire-safety interlocks, and facility-standard compliance.

Skilled in customer-facing field support, resolving both equipment and process issues, interpreting customer-side analysis, and improving satisfaction through practical, specification-aware guidance.

Led development of a novel computer-vision ASIC with a French startup, serving as product manager and driving specification alignment, technical integration, and customer communication. This ASIC became the core of a stereo-vision passenger-counter system deployed in 20,000+ units across Asia. Additional experience includes real-time embedded systems, FPGA-based logic verification, embedded C/C++, and global engagement across Europe and Asia.

Brings a unique blend of semiconductor expertise, equipment-installation know-how, cross-functional leadership, and safety-driven field experience—ready to contribute immediately.

Core Competencies

Semiconductor Process & Devices – CVD/ALD, plasma etch, Co-salicide, SOI CMOS, FeRAM, RTP, interface engineering **Failure Analysis & Metrology** – TEM, FIB, SEM, EDS, XRD, XRF, AFM; defect root-cause analysis **Equipment Installation & Facilities** – Utility coordination, multi-vendor construction, tool move-in/hook-up/bring-up, acceptance testing **Safety & Reliability** – Work-site safety, tool load-distribution/anchoring, gas/fire alarms, interlocks, facility compliance	**Real-time Embedded Systems** – Timing/sequence control, state-transition logic, frame-synchronized processing **Computer Vision & LSI** – Image-analysis ASICs, FPGA prototyping, embedded C/C++, real-time video analytics **Product Management** – Specification alignment, field deployment, technical sales, global support **Leadership & Collaboration** – Joint development with overseas partners, project leadership, product promotion

Technical Skills / Tools

Analytical Instruments – TEM, FIB, SEM, EDS, XRD, XRF, AFM; clean-bench operation; analytical specimen preparation	**Electrical / Device Measurement** – Wafer probers (manual, auto), oscilloscopes **Design & Engineering** – Xilinx FPGA/Vivado, Embedded C/C++, Python, Serial communication,

Manufacturing Tools & Metrology – CVD/ALD, spin coaters, plasma etchers, RTP, wafer-cleaning; CD-SEM, particle counters, ellipsometry/reflectometry, inline XRF, oblique-illumination inspection	real-time embedded systems, PCB design (Altium/Cadlus), video signal handling, image sensors (HDR/NIR/FIR/ToF), image processing, AI-based image recognition

Professional Training

- ISO-compliant safety training (cleanroom operation, chemical handling, high-pressure gas safety).
- ASM headquarters hardware/software training; on-site tool-installation and maintenance training at OKI Electric's Hachioji fab.
- Vendor-provided training for new semiconductor tools (process engineering, field-service procedures, equipment operation).
- Manufacturer-provided training for analytical instruments (TEM, FIB, SEM, EDS, XRD, XRF, AFM).

Work Experience

BVS-TECH HONG KONG (SELF-EMPLOYED) NOV 2016 – PRESENT

Founder / Independent Consultant – Computer Vision & Embedded Systems

- Founded BVS-Tech Hong Kong to support deployment of stereo-vision passenger-counter systems for bus applications in China.
- Responsible for device design, counting algorithms, inter-device communication, firmware development, reliability testing, and field validation under harsh outdoor conditions.

Stereo-Vision Passenger Counter – Technical Highlights

- Designed and implemented the full hardware–firmware stack: ceiling mounted camera module + custom image-analysis ASIC, controlled via serial communication with the vehicle's onboard controller (destination display, announcements, mobile data link).
- Developed the complete counting algorithm, command/response protocol, and firmware. Implemented real-time, frame-synchronized stream analysis with parameters written during blanking periods and results read at frame boundaries.
- Added multi-frame detection logic, adaptive thresholds, and door-open/close tracking to prevent miscounts. Optimized performance using extensive simulation across diverse lighting and weather conditions, achieving **95%+ counting accuracy** in real world operation.
- **Applied timing- and sequence-control concepts** analogous to semiconductor manufacturing equipment, including synchronized stream processing, conditional state transitions, interlock-like behavior, and timing-critical parameter updates implemented directly in firmware.

Deployment & Customer Engagement

- Lived on site to coordinate both device-side and bus-side integration, defining installation procedures and operational workflows.
- Adopted the custom image-analysis ASIC I had developed as product manager at Lapis, and commercialized it as the core of the stereo-vision passenger-counter device.

- Successfully shipped **20,000+ units**, ensuring stable operation in real-world bus environments.
- Since 2020, shifted focus to Japanese customers due to COVID-19, promoting computer-vision solutions (custom LSI and AI-based software) and achieving deliveries to **SUBARU Corporation** and other clients.

LAPIS SEMICONDUCTOR CO., LTD. APR 1998 – OCT 2016

(formerly OKI Semiconductor; Semiconductor Division of OKI Electric Industry, acquired by ROHM)

Senior Engineer / Project Lead – Computer Vision & Custom LSI Development (Mar 2007 – Oct 2016)

Joint Development of Novel Image-Analysis LSI (with BVS, France)

- Led a joint development project with French startup BVS, working directly with CEO Patrick Pirim (now CTO of AnotherBrain) and core engineering staff.
- Completed a three-month residency at BVS in Paris to master the company's proprietary stream-based video-analysis logic, simulation tools, and application-level design.
- Maintained long-term technical collaboration, refining application concepts and aligning architectures between both companies.

Custom LSI Development on OKI ASIC Platform

- Served as ASIC product manager, coordinating specification alignment with BVS and leading integration of their logic architecture into OKI's microcontroller-embedded ASIC platform.
- Oversaw prototype LSI development, bring-up, debugging, and customer evaluations.
- The resulting custom image-analysis ASIC was later adopted and commercialized in BVS-Tech's stereo-vision passenger-counter system.

FPGA-based Logic Verification & Demo Application Development

- Verified BVS logic using FPGA evaluation kits and developed multiple real-time demo applications, including surveillance, pedestrian detection, vehicle detection, and gaming interfaces.
- Implemented algorithms in C/C++, using assembly for low-level debugging when required.

Stream-Based Video Analysis Architecture

- Worked with a logic architecture that extracts multiple feature streams from input video (luminance, saturation, hue, motion, velocity, edge strength, edge angle, curvature, etc.).
- Utilized 12 configurable analysis cells to evaluate spatial distributions and detect regions of interest.
- Combined multiple feature streams using logical operations (AND/OR/NOT/XOR) to define complex detection conditions.
- Achieved fully hardware-based, real-time processing synchronized with video input, minimizing enabling per-frame reconfiguration and minimizing MCU load.

Team Leadership & Customer Engagement

- Led an 8-member team responsible for logic verification, development-environment setup, demo-kit creation, and customer-specific demonstrations.
- Conducted technical promotions and demonstrations for individual customers and partner companies.

Stereo-Vision Passenger Counter (2011–2014)

- Initiated and developed a stereo-camera-based passenger counter prototype for bus applications in Anhui Province, China.
- Invented a hardware method to generate disparity streams directly from stereo input, simplifying optical alignment and enabling real-time 3D object detection.
- Resulted in international patent:
  - ✓ **WO2011/115142 – Image Processing Device, Method, Program and Storage Medium.**
- Evaluated potential applications such as rear-view collision-avoidance systems.

Technical Sales – Battery Monitoring LSI (2013–2016)

- Served as European technical-sales lead for Li-ion battery monitoring LSIs (BMS).
- Conducted 4–5 business trips per year to Europe, visiting Bosch Group, SAFT, and other major customers with local sales teams.
- Achieved design-in success with **Pellenc (France)** for battery-powered agricultural machinery.

Process Engineer / Senior Engineer – Semiconductor Process & Device Development (Apr 1998 – Mar 2007)

Failure Analysis & Materials Evaluation

- Joined the analysis team as an immediate contributor, performing defect analysis and materials evaluation for semiconductor processes.
- Conducted advanced failure analysis using **TEM, FIB, SEM, EDS, XRD, XRF, AFM**, and other techniques to identify process-induced defects and material issues.

Co Salicide & SOI Device Development

- Participated in SOI device development and invented **a breakthrough Co salicide process** for fully-depleted SOI devices.
- Used TEM and interface analysis to clarify the mechanism and demonstrate the electrical benefits of the new process.
- Contributed to multiple high-impact publications, including:
  - ✓ Advanced Co salicide technology for Sub-0.20 µm fully-depleted SOI devices, *JJAP* 40 (2001).
  - ✓ Fully-depleted SOI CMOSFETs with the fully-silicided source/drain structure, *IEEE TED* 49 (12), 2002.

Equipment Installation & Factory Integration

- Managed **three full equipment-installation projects** at the OKI Electric Hachioji fab in Tokyo, including tools from **ASM**, **Aixtron**, and **Primaxx** (US CVD startup).
- Coordinated factory-side utility preparation (electrical, gas, exhaust, vacuum, cooling water), multi-vendor construction work, and tool move-in, hook-up, and bring-up.
- Conducted acceptance testing; for the Primaxx CVD tool, identified critical non conformities and led the full decommissioning and removal process.
- Ensured work site safety and operational reliability through gas detection systems, fire safety interlocks, equipment anchoring/load-distribution planning, and compliance with facility safety standards.

FeRAM Project (OKI / Sony Joint Project)

- Selected, introduced, and managed deposition tools for ferroelectric-capacitor and barrier films:
  - ✓ **ASM Al_2O_3 barrier-film deposition system**
  - ✓ Aixtron SBT (Sr,Bi,Ta oxide) ferroelectric-film deposition system
- Designed and managed capacitor-formation processes, including deposition, RTP and after-etch recovery.
- Evaluated capacitor characteristics and read/write-circuit performance.
- Presented results at IEDM as part of the OKI/Sony collaboration.
  - ✓ A novel stack capacitor cell for high-density FeRAM compatible with CMOS logic, *IEDM Digest*, 2002.

Plasma Etch & Defect Mechanisms

- Investigated proton-channeling-induced defects at the bottom of ultrahigh-aspect-ratio contact holes during plasma etching.
  - ✓ Proton channeling into the Si substrate at the bottom of ultrahigh-aspect-ratio contact holes during plasma etching, *Thin Solid Films* 374 (2000).

JAPAN SCIENCE AND TECHNOLOGY AGENCY APR 1997 – MAR1998

Research Fellow, ERATO TANAKA Solid Junction Project

- Performed advanced interface characterization using Transmission Electron Microscopy (TEM) and Focused Ion Beam (FIB) techniques, focusing on atomic-scale analysis of thin-film and multilayer structures.
  - ✓ Nanoscopic analysis of a Ag-Cu-Ti/sapphire interface, *Materials Science Forum* (1999).
- Developed cross-sectional sample preparation and analytical methodologies that improved reproducibility and accuracy in interface evaluation.
- Collaborated with university laboratories and national research teams to investigate diffusion behavior, defect formation, and material-degradation mechanisms.
- Contributed to JST-sponsored intellectual-property creation, including patent filings related to interface engineering and thin-film process technologies
  - ✓ JP Patent Application Hei 10-187681 (1998), Joining structure characterized by Cu–Al–O and Ti-based reaction products at the Al_2O_3 / Cu–Ti brazed interface.

Education

Ph.D. (Engineering), Materials Science

The University of Tokyo, Graduate School of Engineering (APR 1991 – MAR 1997)

- Conducted research on atomic-scale grain-boundary and interface structures using transmission electron microscopy (TEM).
- Responsibilities included cross-section and interface sample preparation, TEM specimen preparation, TEM operation, and structural analysis and interpretation.

B.Eng., Materials Science

The University of Tokyo, Faculty of Engineering (APR 1987 – MAR 1991)

Selected Publications

- T. Ichimori, C. Iwamoto, S.-I. Tanaka, "Nanoscopic analysis of a Ag–Cu–Ti/sapphire interface," *Materials Science Forum*, vols. 294–296, pp. 337–340, 1999.
- T. Ichimori *et al.*, "Proton channeling into the Si substrate at the bottom of ultrahigh-aspect-ratio contact holes during plasma etching," *Thin Solid Films*, vol. 374, pp. 228–234, 2000.
- T. Ichimori *et al.*, "Co salicide technology for sub-0.15 µm FD-SOI and beyond: super-flat silicide and fully-silicided source/drain structure," *IEEE International SOI Conference*, 2000.
- T. Ichimori *et al.*, "Advanced Co salicide technology for Sub-0.20 µm fully-depleted SOI devices," *Jpn. J. Appl. Phys.*, vol. 40, pp. 2881–2886, 2001.
- T. Ichimori *et al.*, "Structural study of single {111} facetted $CoSi_2$/Si interface incorporated in a SOI MOSFET," *Jpn. J. Appl. Phys.*, vol. 40, pp. L1019–L1021, 2001.
- T. Ichimori *et al.*, "Fully-depleted SOI CMOSFETs with the fully-silicided source/drain structure," *IEEE Trans. Electron Devices*, vol. 49, no. 12, 2002.
- F. Ichikawa, T. Ichimori *et al.*, "Fully depleted SOI process and device technology for digital and RF applications," *Solid-State Electronics*, vol. 48, pp. 999–1006, 2004.
- T. Hayashi, T. Ichimori *et al.*, "A novel stack capacitor cell for high density FeRAM compatible with CMOS logic," *IEDM Digest*, 2002.

Selected Patents (Japan / US / WO)

US Patents

- **Instruction Beam Detection Apparatus and Method of Detecting Instruction Beam**
  US 9,407,305 B2, Aug. 2016.
  Inventor: Takashi Ichimori.
- **Structure of a Field Effect Transistor Having Metallic Silicide and Manufacturing Method Thereof**
  US 7,479,682 B2, Jan. 2009.
  Inventors: Norio Hirashita, Takashi Ichimori.
- **Method for Fabricating a Semiconductor Device Having a Metallic Silicide Layer**
  US 6,274,470 B1, Aug. 2001.
  Inventors: Takashi Ichimori, Norio Hirashita.

- **Memory Cell Structure and Semiconductor Memory Device**
  US 7,405,439 B2, Jul. 2008.
  Inventor: Takashi Ichimori.
- **Ferroelectric Memory and Method of Manufacturing Same**
  US 2006/0054949 A1, Mar. 2006.
  Inventor: Takashi Ichimori.
- **SOI MOS Field Effect Transistor and Manufacturing Method Therefor**
  US 6,750,088 B2, Jun. 2004.
  Inventors: Norio Hirashita, Takashi Ichimori.

WO Patent

- **Image Processing Device, Method, Program and Storage Medium**
  WO 2011/115142 A1, Sept. 2011.
  Inventor: Takashi Ichimori.

JP Patent

- **Joining structure characterized by Cu–Al–O and Ti-based reaction products at the Al_2O_3 / Cu–Ti brazed interface**
  JP Hei 10-187681 (1998).
  Inventor: Takashi Ichimori.

Languages

- Japanese: Native
- English: Business-level / Fluent
- Mandarin Chinese: Beginner